THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte LOUIS LU-CHEN HSU, CHANG-MING HSIEH, and SEIKI OGURA

Appeal No. 95-3637
Application 07/968,736[1]

ON BRIEF

Before JERRY SMITH, FLEMING and LEE, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision under 35 U.S.C. § 134 from the final rejection of claims 1-4, and 9-15. Claims 5-8 have been withdrawn from consideration. Claim 16 has been allowed.

References relied on by the Examiner

Lee	5,041,886	Aug. 20, 1991

[1] Application for patent filed October 30, 1992.

The Rejections on Appeal

Claims 1-4 and 9-15 stand finally rejected under 35 U.S.C. § 103 as being unpatentable over Lee.

The Invention

The invention is directed to an integrated EEPROM wherein the select and floating gates are each formed from polysilicon sidewalls. Claims 1 and 9 are independent claims and are reproduced below:

1. An EEPROM cell comprising a dual-gate transistor having a select gate, a floating gate and a control gate disposed on top of the floating gate, said gates being disposed above a channel and between a source and drain, said select gate being separated vertically from said channel by a gate oxide, said floating gate being separate vertically from said channel by a tunnel oxide and said control gate being separated vertically from said floating gate by a second layer of insulator; characterized in that:

said select and floating gates are each formed from polysilicon sidewalls and are separated horizontally by a thin vertical insulating member.

9. An integrated circuit EEPROM comprising:

input/output means for passing data into and out from said EEPROM;

voltage generating means for generating a predetermined program voltage;

voltage steering means for directing said program voltage along predetermined program paths in said circuit; and a memory array comprising;

a set of dual-gate field effect transistor memory cells, each dual-gate transistor comprising a select gate, a control

gate and a floating gate disposed above a channel and between said common source and a drain, said select gate being separated vertically from said channel by a gate oxide, said floating gate being separated vertically from said channel by a tunnel oxide and said control gate being separated vertically from said floating gate by a second layer of insulator, characterized in that;

said select and floating gates are each formed from polysilicon sidewalls having a vertical side and are separated horizontally by a thin vertical insulating member adjacent said vertical side of said select and floating gates.

Opinion

We sustain the rejection of claims 1, 3, 9, 11, 13 and 15, but not the rejection of claims 2, 4, 10, 12 and 14.

Our opinion is based only on the arguments presented by the appellants in their briefs. Arguments not raised in the briefs are not before us, are not at issue, and are considered waived.

As argued by the appellants, the sole difference between the subject matter of independent claims 1 and 9, and that disclosed by Lee is that **both** the select and floating gates of the claimed invention are "formed from polysilicon sidewalls," not just the select gate.

The appellants state (Br. at 4):

> The term "sidewall" has been used in the application consistent with standard terminology in the art to refer to a generally vertical member that is the residue of a conformal layer after horizontal portions have been etched in an anisotropic process.

However, the appellants fall short of asserting that the term "sidewall" has an established meaning in the art that can "only" have the meaning urged by the appellants and which makes unreasonable "any other" interpretation. That the term "sidewall" may frequently or usually take on the meaning urged by the appellants does not mean it has no other reasonable interpretation. Here, the appellants' specification does not specially define the term but merely uses it descriptively. Other meanings are not excluded by the specification.

Even if the appellants had asserted that the term "sidewall" has an established meaning in the art that can

"only" have the meaning urged by the appellants and no other reasonable interpretation, no evidence has been submitted in support of the assertion. Mere argument of counsel does not take the place of evidence. In re Langer, 503 F.2d 1380, 1395, 183 USPQ 288, 299 (CCPA 1974). See also Meitzner v. Mindick, 549 F.2d 775, 782, 193 USPQ 17, 22 (CCPA 1977), cert. denied, 434 U.S. 854, 195 USPQ 465 (1977). We decline to regard argument as fact, especially an argument not actually made by the appellants, i.e., that the meaning for "sidewall" as urged by the appellants is the **only** reasonable meaning and that the established meaning for "sidewall" **excludes or prohibits** the broader reading by the examiner.

The examiner is interpreting the term "sidewall" according to its ordinary meaning in the English language. We agree with the examiner that the structure shown in Lee's Figures 15A and 16A includes a vertical surface of silicon oxide 105 between and immediately adjacent the select gate on one side thereof and the floating gate on the other. Claim terms are properly interpreted during examination based on their broadest reasonable interpre- tation in light of the

specification. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989); In re Yamamoto, 740 F.2d 1569, 1571, 222 USPQ 934, 936 (Fed. Cir. 1984); In re Pearson, 494 F.2d 1399, 1404, 181 USPQ 641, 645 (CCPA 1974); In re Prater, 415 F.2d 1393, 1404, 162 USPQ 541, 550 (CCPA 1969). In our view, it is reasonable for the examiner to regard select gate 30 and floating gate 10 in Lee as sidewalls to the vertical silicon oxide surface existing therebetween, in the absence of evidence sufficient to demonstrate for the term "sidewall" an established meaning in the art which does not permit or allow the simple interpretation by the examiner.

Finally, even if the appellants have established that the term "sidewall" has the meaning urged on page 4 of their brief, and that that is the only reasonable interpretation of the term, it would not help their case, since structural claims generally are not limited by process steps used in the making of the structure. As is specifically stated by the Federal Circuit in In re Thorpe, 777 F.2d 695, 697, 227 USPQ 964, 966 (1985):

> [E]ven though product-by-process claims are limited by and defined by the process, determination of

> patentability is based on the product itself. [Citations omitted.]
>
> The patentability of a product does not depend on its method of production. In re Pilkington, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969). If the product in a product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. In re Marosi, 710 F.2d 799, 803, 218 USPQ 289, 292-93 (Fed. Cir. 1983); Johnson & Johnson v. W.L. Gore, 436 F.Supp. 704, 726, 195 USPQ 487, 506 (D. Del. 1977); see also In re Fessman, 489 F.2d 742, 180 USPQ 324 (CCPA 1974).

Thus, different manufacturing process steps do not serve to distinguish resulting structures which are otherwise the same. The appellants have failed to demonstrate that in the absence of the process step of forming the select and floating gates as the vertical residue of a conformal layer after the horizontal portions of the conformal layer have been removed by anisotropic etching, the claimed polysilicon select and floating gates are any different from those of Lee.

For the foregoing reasons, we sustain the rejection of claims 1, 3, 9, 11, 13 and 15.

As for dependent claims 2, 4, 10, 12 and 14, the examiner is incorrect that the appellants have grouped them together

with independent claims 1 and 9. Indeed, on page 3 of the brief, the appellants specified two separate groups for argument, and on page 6 the appellants advanced arguments for claims 2, 4, 10, 12 and 14 as a second group.

The examiner has failed to address and account for the claimed features of dependent claims 2, 4, 10, 12 and 14. The initial burden is on the examiner to establish a prima facie basis to reject the claims. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The examiner must provide a factual basis to support an obviousness conclusion. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968) (The examiner may not resort to speculation, assumptions, or hindsight reconstruction); In re Lunsford, 357 F.2d 385, 391, 148 USPQ 721, 725 (CCPA 1966) (The provisions of section 103 must be followed realistically to develop the factual background against which the section 103 determination must be made); In re Freed, 425 F.2d 785, 787, 165 USPQ 570, 571 (CCPA 1970) (A determination of obviousness must be based

on facts and not on unsupported generalities). Accordingly, the rejection of dependent claims 2, 4, 10, 12 and 14 cannot be sustained.

Conclusion

The rejection of claims 1, 3, 9, 11, 13 and 15 under 35 U.S.C. § 103 as being unpatentable over Lee is affirmed.

The rejection of claims 2, 4, 10, 12 and 14 under 35 U.S.C. § 103 as being unpatentable over Lee is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JERRY SMITH Administrative Patent Judge	)
MICHAEL R. FLEMING Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES

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